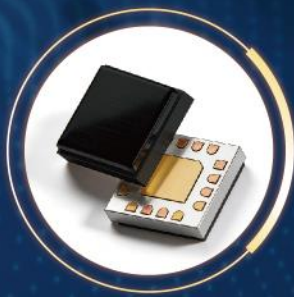
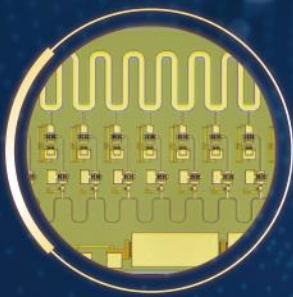


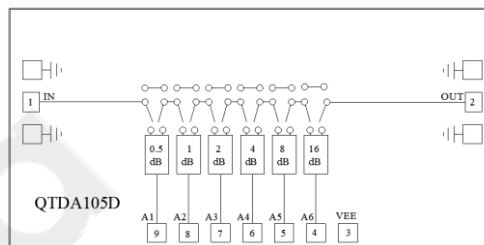
Wideband GaAs & GaN MMIC



Features

- ◆ Ultra Wideband Performance
- ◆ Low Insertion Loss
- ◆ Wide Attenuation Range
- ◆ High Attenuation Accuracy

Functional Block Diagram



Description

The QTDA105D is a broadband GaAs MMIC 6-bit digital attenuator operating from DC to 30 GHz. It features a total attenuation of 31.5 dB with high accuracy ± 0.6 dB and a typical insertion loss of 5.0 dB. The chip is TTL-controlled with a -5 V power supply and offers fast switching speed. Both the input and output ports are matched to 50 Ω , and the surface is protected by a passivation layer.

Electrical Specifications :TA = +25°C, VEE = -5V, VCTL = 0/ +5V

Parameters	Min	Typ	Max	Min	Typ	Max	Units
Frequency	DC		20	20		30	GHz
Insertion Loss		5.0	5.5		6.3	6.8	dB
Attenuation Range		31.5			32		dB
Attenuation accuracy (Referenced to Insertion Loss)		± 0.6			± 1.5		dB
Input Return Loss (RF1 & RF2, All Atten States)		-14			-13		dB
Output Return Loss (RF1 & RF2, All Atten States)		-15			-16		dB
Input P1dB		23			24		dBm
IIP3		35			36		dBm
Switching Characteristics	tRISE, tFALL (10/90% RF)	60			60		ns
	tON/tOFF (50% CTL to 10/90% RF)	90			90		ns

Absolute Maximum Ratings

Parameter	Rating
RF Input Power (RFIN)	+24dBm
VEE	-6 Vdc
Channel Temperature	175°C
Operating Temperature	-55°C to +85°C
Storage Temperature	-65°C to +150°C
ESD Sensitivity (HBM)	Class 1A

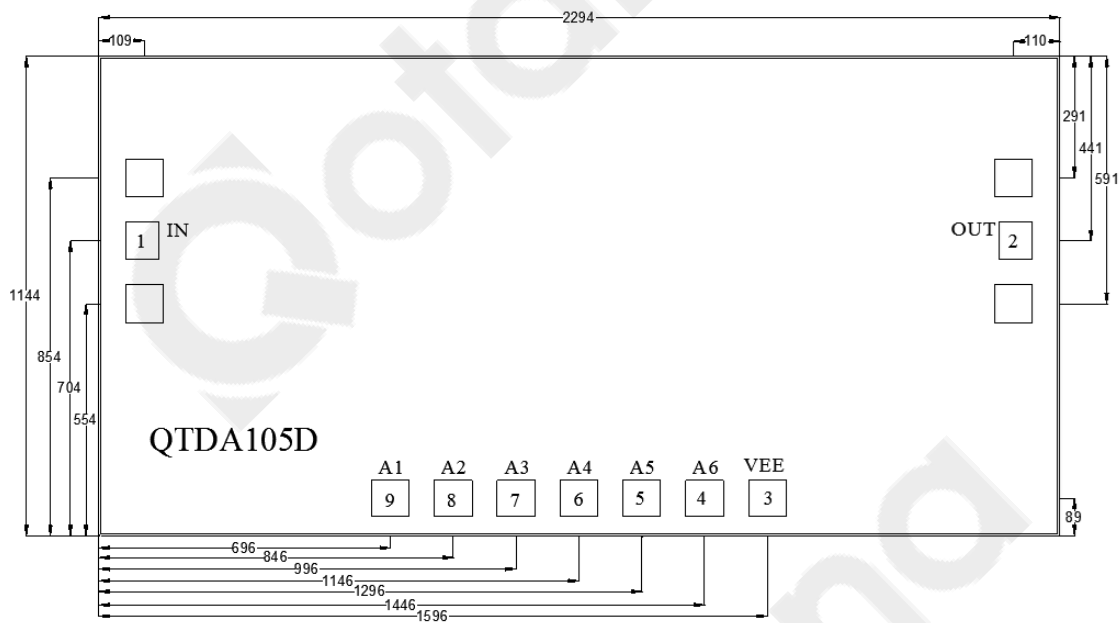
ESD Caution

	ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS
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Ordering Information

Part No.	Package	Description
QTDA105D	Die	DC-30GHz 6-Bit Digital Attenuator

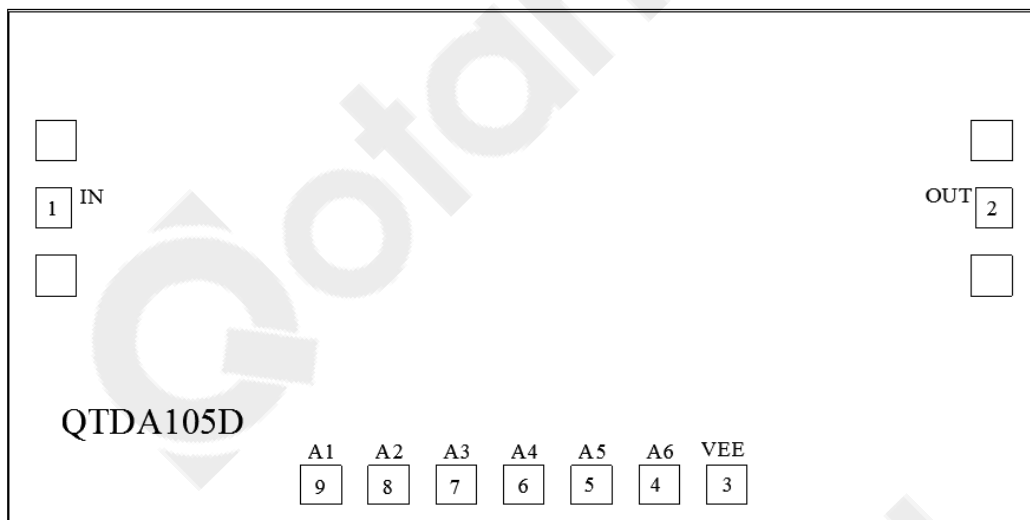
Outline Drawing: All Dimensions in μm



Notes:

- 1. Die is 100 microns thick
- 2. DC bond pads are 90 x 87 microns
- 3. RF bond pads are 80 x 90 microns

Pad Description

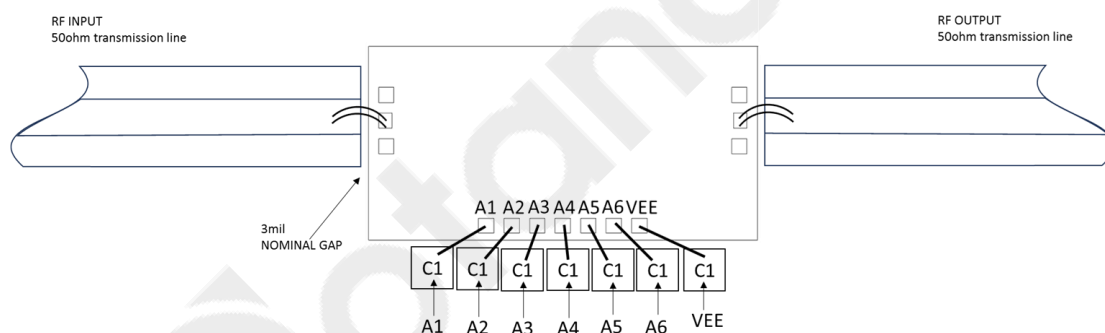


Notes:

- ◆ 1. No connection required for unlabeled pads
- ◆ 2. Backside and bond pad metal: Gold

Pad	Function	Description
1	IN	This pad is DC coupled and matched to 50 Ohm. Blocking capacitors are required if RF line potential is not equal to 0V.
2	OUT	This pad is DC coupled and matched to 50 Ohm. Blocking capacitors are required if RF line potential is not equal to 0V.
3	VEE	Negative bias -5V.
4, 5, 6, 7, 8, 9	A1, A2, A3, A4, A5, A6	Control pad, see truth table and control voltage table.
Backside	Ground	Connect to RF / DC ground

Assembly Drawing



Item	Value	Part No	Manuf.
C1	100pF	CSM-140-15X15X4-G-101-K	Knowles Dielectric Labs

Truth Table

Control Voltage Input							Attenuation State IN-OUT
A1	A2	A3	A4	A5	A6	VEE	
0	0	0	0	0	0	-5V	Reference IL
1	0	0	0	0	0	-5V	0.5dB
0	1	0	0	0	0	-5V	1dB
0	0	1	0	0	0	-5V	2dB
0	0	0	1	0	0	-5V	4dB
0	0	0	0	1	0	-5V	8dB
0	0	0	0	0	1	-5V	16dB
1	1	1	1	1	1	-5V	31.5dB

Bias Voltages & Currents

VEE	-5V @ 4mA (Typ)
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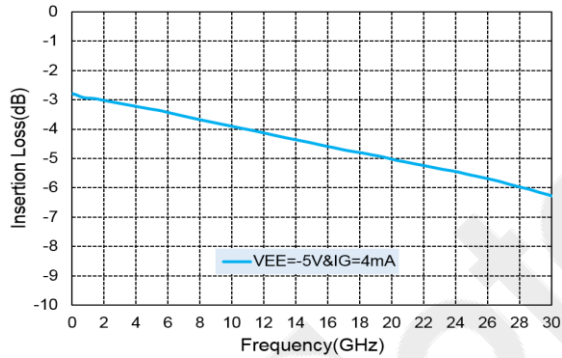
Control Voltage

State	Bias Condition
Low(0)	0 to 0.8V @ 1 μ A (Typ)
High(1)	2 to 5V @ 1 μ A (Typ)

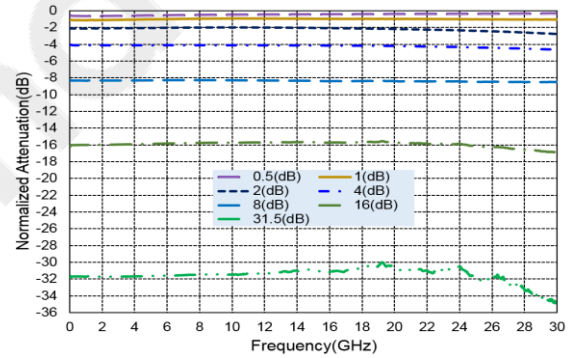
Typical Performance Plots

 $T_A = +25^{\circ}\text{C}$

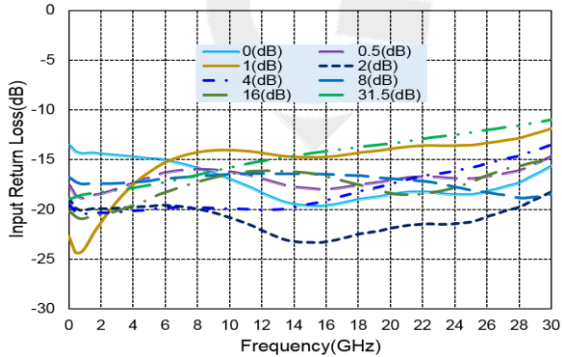
Insertion Loss vs. Frequency



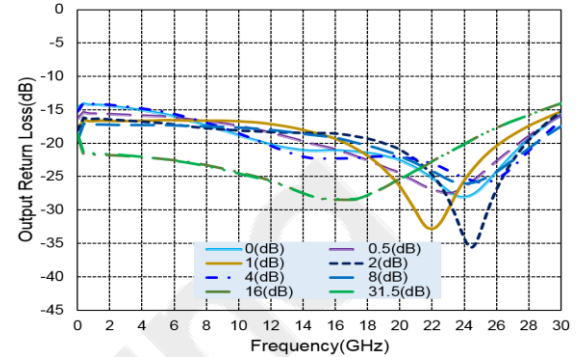
Normalized Attenuation vs. Frequency



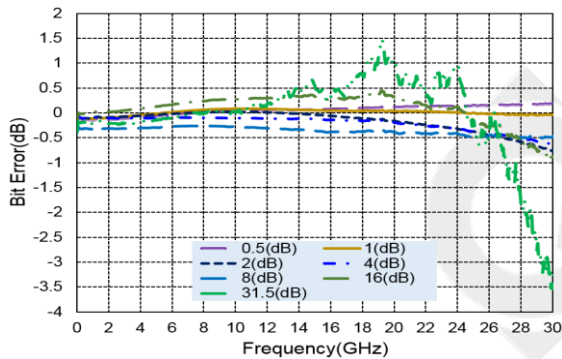
Input Return Loss vs. Frequency



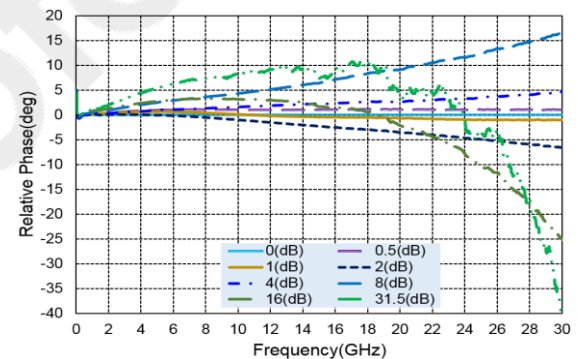
Output Return Loss vs. Frequency



Bit Error vs. Frequency



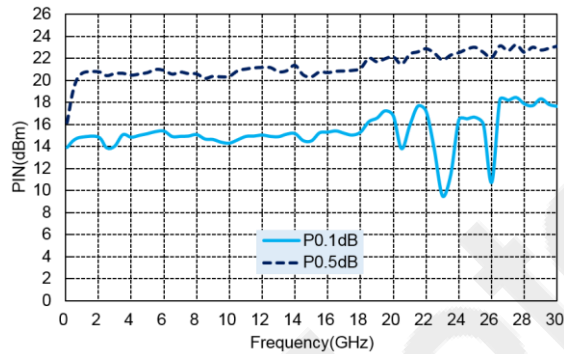
Relative Phase vs. Frequency



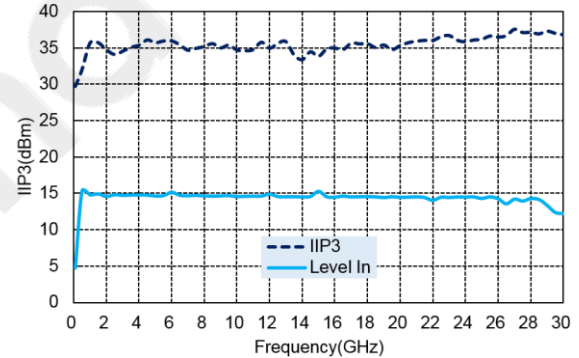
Typical Performance Plots

 $T_A = +25^{\circ}\text{C}$

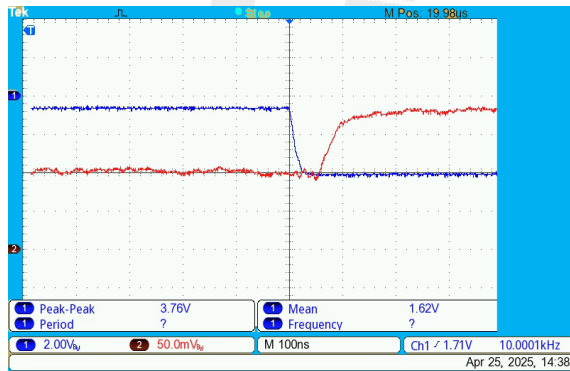
Pin vs. Frequency



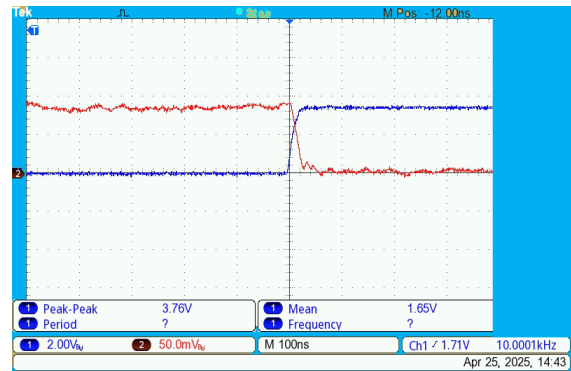
IIP3 vs. Frequency



Switching Rise Time



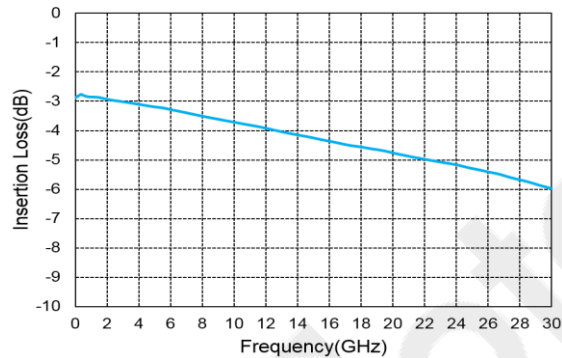
Switching Fall Time



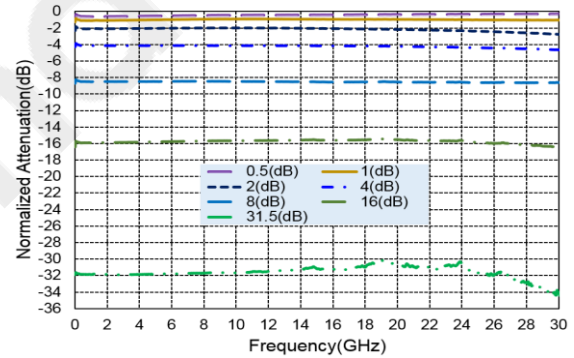
Typical Performance Plots

 $T_A = -40^{\circ}\text{C}$

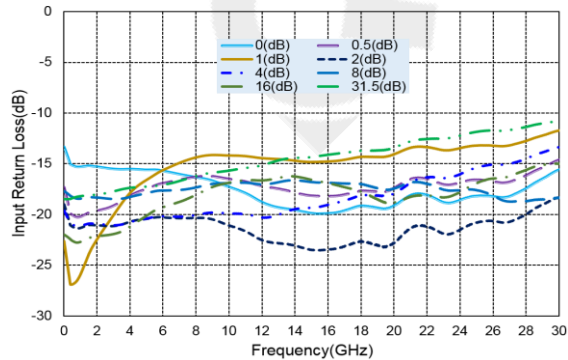
Insertion Loss vs. Frequency



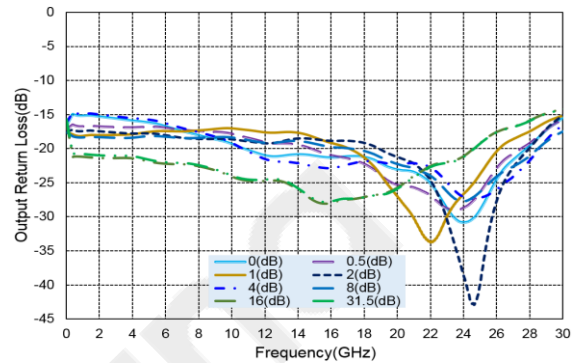
Normalized Attenuation vs. Frequency



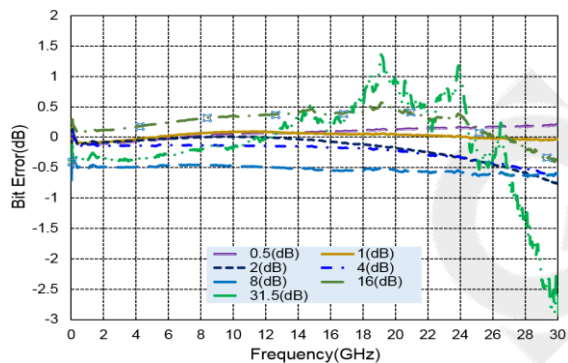
Input Return Loss vs. Frequency



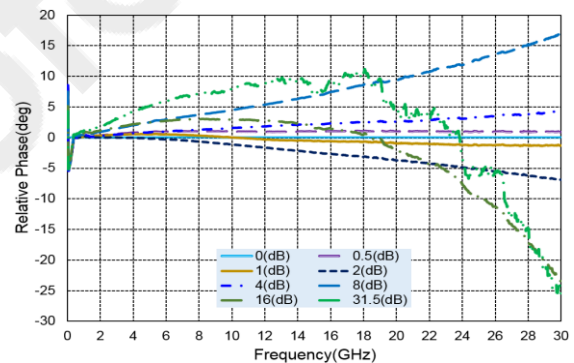
Output Return Loss vs. Frequency



Bit Error vs. Frequency



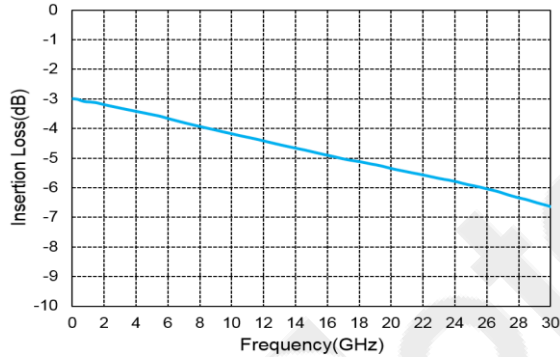
Relative Phase vs. Frequency



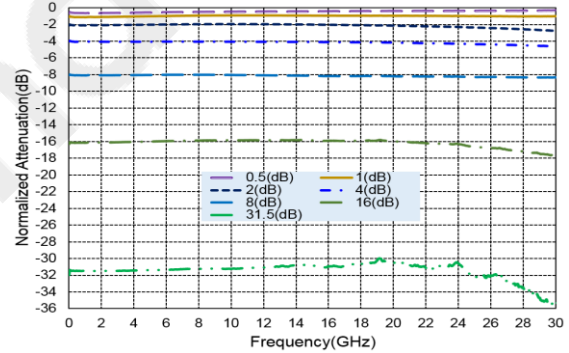
Typical Performance Plots

 $T_A = +85^{\circ}\text{C}$

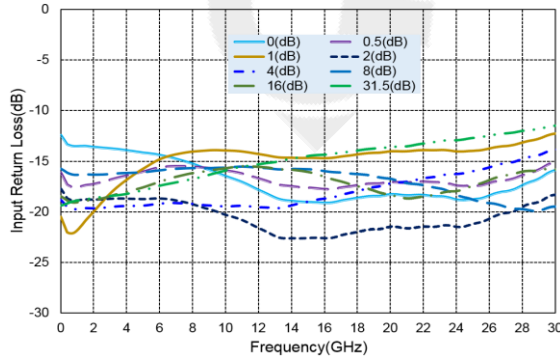
Insertion Loss vs. Frequency



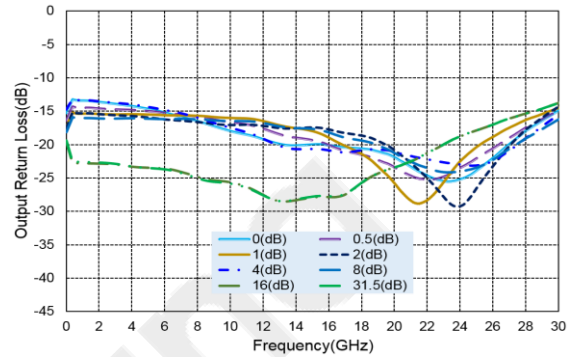
Normalized Attenuation vs. Frequency



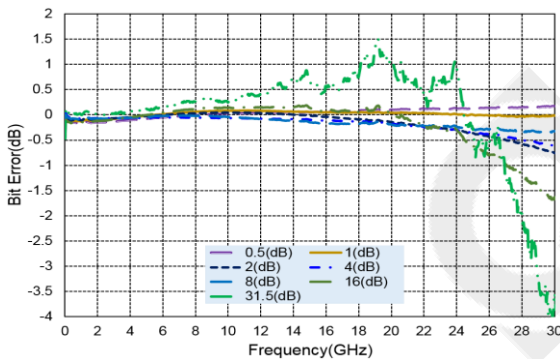
Input Return Loss vs. Frequency



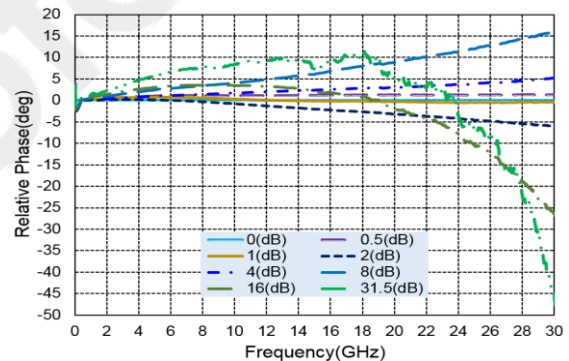
Output Return Loss vs. Frequency



Bit Error vs. Frequency



Relative Phase vs. Frequency



Assembly Instructions

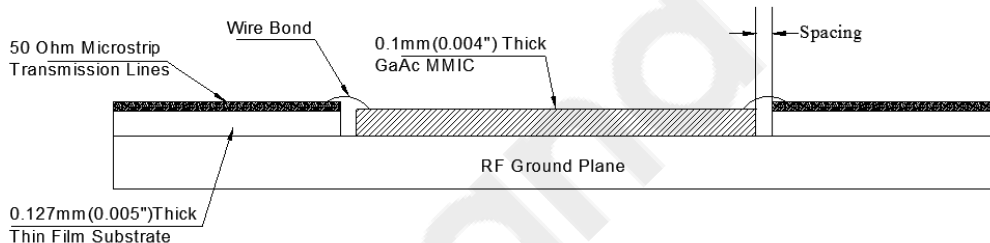


Figure1

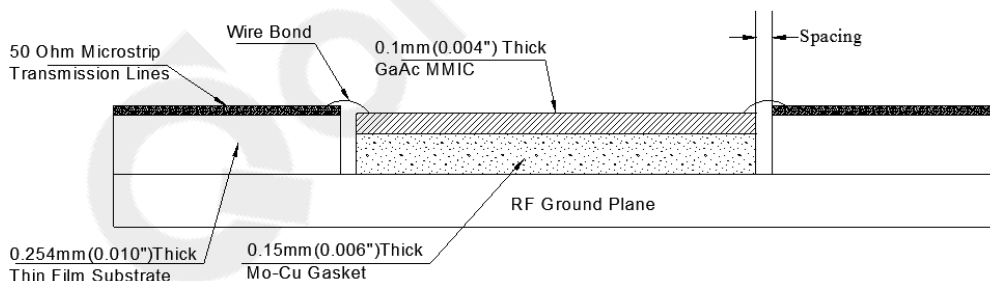


Figure2

- ◆ The small signal die can be bonded with conductive adhesive.
- ◆ It is recommended to use AuSn alloy for the power amplifier die, and weld it on a molybdenum copper substrate in the nitrogen or nitrogen-hydrogen atmosphere using the eutectic welding process. The time at temperatures above 320°C should not exceed 20 seconds.
- ◆ Thermosonic wedge bonding is an excellent interconnection technology.
- ◆ In general, the 25μm gold wire will be used to connect the die and microstrip lines. But if the pad size is less than 80μm, the 18μm gold wire is the best choice.
- ◆ During the process of assembling, the spacing should be between 0.06mm and 0.15mm when the frequency of the die is below 40GHz, but if the frequency is over 40GHz, the commend spacing is between 0.03mm and 0.06mm.
- ◆ You have to make sure that the surface of the die and microstrip line are almost keep in the same horizontal.